Next Generation of Poly-Si TFT Technology: Material Improvements and Novel Device Architectures for System-On-Panel (SOP)

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Abstract

In this paper we present advances in poly-Si TFT technology driven by the demands of the next SOP generations. Improved Si crystallization technology enables significant reductions of the variability in TFT characteristics, due to improved defect control. Advanced gate insulator technology allows thickness scaling of the gate dielectric film (concomitant to device scaling) without loss of performance or reliability. New plasma deposition technology developed and optimized at SLA provides for such improvements due to virtual elimination of inadvertent plasma damage in the dielectric film. Research on novel device architectures enables the integration of such process improvements with device structures that complement and customize device performance according to function. SLA's research and development will be the main thrust behind the 3rd SOP generation and the continued development of "one-of-a-kind" display products at SHARP.

この論文では，Poly-Si TFT 技術の進展について紹介します。SLA（シャープアメリカ研究所）では，次世代 SOP を実現すべく，Poly-Si TFT 技術の研究開発を進めています。Si 結晶化技術の向上により，欠陥制御性が改善され，TFT 特性のばらつきが低減されます。アドバンスト・ゲート絶縁膜技術により，デバイス微細加工深化に伴うゲート絶縁膜の薄膜化が，パフォーマンスや信頼性を損なうことなく可能となります。SLAにて開発した新規プラズマCVD技術は，成膜の際に膜中に生じるプラズマダメージを実質的に除去することにより膜質の改善を行います。新規デバイス・アーキテクチャの研究により，これら新規プロセス技術とデバイス構造とを統合することが可能となります。これにより実現すべき機能に対し，必要なデバイス性能を作り込む事ができます。SLA における研究開発は，次世代SOP開発，及びSharpオンリーワン・ディスプレイ商品開発への主要な推進力となります。

Intorduction

Polysilicon thin-film-transistors (TFT) are key building blocks for active-matrix-driven flat panel displays (FPDs). Many studies have demonstrated the ability of poly-Si based transistors to support a variety of functions beyond pixel switching, which has been the traditional role of TFTs in FPD applications [1-2]. Poly-Si material enables the design of smaller TFTs that offer higher current and faster switching characteristics. As a result, pixel-driving circuits can be monolithically integrated on the display substrate [3]. Such integration not only reduces the amount of external interconnections to the panel, but also improves the form-factor of the resulting display. The improved performance of poly-Si TFTs is expected to further yield increasing levels of component integration that will enable the fabrication of unique display systems [4].

To achieve high performance poly-Si TFTs, concomitant improvements at various levels are required. New

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elemental process technology is needed for the formation of high quality critical layers, such as the device active and the gate-insulator layers. In addition, improvements in the device architecture are vital in two aspects: (a) enable the fabrication of sub-µm channel dimensions with technology compatible with LCD manufacturing and (b) provide an additional means to compensate for deficiencies and variation in key layer, material properties.

In terms of active layer, high quality poly-Si microstructure is needed to increase device performance. The crystallization process is a very critical step of the TFT fabrication process, as it needs to satisfy conflicting requirements on material quality and cost and, at the same time, comply with the thermal-budget constraints imposed by the display substrate. Over the past 10 years, laser-based crystallization has been intensely studied and developed for poly-Si TFTs [5-7]. Despite of its shortcomings, laser crystallization is the only technology with the ability to produce very high crystal-quality poly-Si films. This potential has been finally realized, in recent years, by the advent of a variety of laser-based lateral-crystallization technologies that have been shown to yield extremely high-performance transistors with good uniformity [8-10]. However, as the channel dimensions continue to shrink, issues of uniformity emerge even for optimally crystallized Si-films.

In the area of gate insulator, TEOS-based dielectric has been the technology of choice in display manufacturing. As in the case of VLSI, device scaling in poly-Si TFTs necessitates reductions in the gate insulator thickness. With the GI thickness gradually decreasing to 50 nm and beyond, TEOS technology seems incapable of meeting the challenge, in terms of maintaining high quality for increasingly thinner GI layer.

Although improvements in elemental process technology can substantially elevate device performance, further complications exist, specific to LCD operations. For example, device scaling into the sub-µm domain is more challenging due to limitations in the resolution of lithography equipment that are capable of handling large substrates. Additionally, restrictions in the control of junction depth and doping accuracy are more prevalent in TFT technology due to limitations in process technology for doping and activation, imposed by equipment and substrate constraints. As a result, novel TFT device architectures are also needed to overcome such challenges.

Our group at Sharp Labs of America has been working on next generation poly-Si TFT materials and device technology. In this work we present recent developments in key elemental process technology and TFT device architecture, consistent with the issues of performance and scaling for SOP applications.

1. SYSTEM-ON-PANEL REQUIREMENTS

Fig.1 shows the anticipated evolution of poly-Si technology development and its impact on the degree of on-panel integration (adopted from ref. [2] and other published information). From the point of view of device performance, keywords are high speed and low power consumption. From the point of view of system, keywords are high resolution and added value/functionality.

To achieve high speed, significant advances are needed in carrier mobility and fine lithography. For low power consumption, low and centered (between nMOS and pMOS device types) threshold voltage is needed with exceptionally tight distribution. Such characteristics will enable the realization of ultra-high resolution displays with on-board processing capability and small form-factor for novel products and applications.

Fig. 2 illustrates the evolution of device design rules, in response to system requirements presented in **Fig. 1**.

Year	2004	2006	2008	2010
SOP Generation (arbitrary)	1st	2nd	3rd	4th
Display Resolution	300ppi	400ppi		
Power Supply	12V	3-5V	1.5-3V	1.5V
TFT Mobility	200-300cm^2/Vs	300-500cm^2/Vs	500cm^2/Vs	
Design Rule	3µm	1.5µm	0.8µm	0.5µm
Logic Frequency	～3MHz	10MHz	20-50MHz	50-100MHz
Key Process Crystallization Gate Insulator Patterning	CGSi	Advanced CGSi Thin GI Fine Patterning	Texture-control CGSi Ultra-thin GI Sub-µm Patterning	
Monolithic Integration	Digital Driver	Timing Generator Photo Sensor Amplifier	Display controller Image processor LN Amplifier	ULC Driver RF Capability Advanced MPU

Fig. 1　Roadmap of poly-Si TFT technology.

Current mass production technologies can apply to 1st SOP generation and be possibly extended to 2nd SOP generation. However, the development of more advanced panels/ systems (i.e. 3rd generation and beyond) requires the development and introduction of new technologies in several key areas of process and device.

Fig. 3 shows a cross-section of a poly-Si TFT device and illustrates the specific requirements for key device layers to meet the technological demands presented in **Fig.2**. Development of new elemental process technologies is needed to achieve high quality active and gate insulator layers in response to the itemized, specific requirements.

2. NOVEL PROCESS TECHNOLOGIES

2.1. Silicon Crystallization

SLA has been developing novel, laser-based crystallization technology, dubbed "advanced-CGSi" (adv-CGSi). adv-CGSi enables significant advances in the microstructural characteristics of poly-Si material, such as long lateral growth length (LGL) and decreased defect density. The process relies on an advanced heating scheme that enables longer solidification time for the laser-irradiated (and molten) Si film. A representative microstructure of such poly-Si film is shown in **Fig.4**.

Using such poly-Si material for the active layer, TFT devices were fabricated and characterized.

Fig.5 summarizes the results, in terms of TFT mobility and threshold voltage. As shown, wide variation in TFT characteristics is observed. The reasons for this variation were carefully analyzed and ascribed to two main causes: (1) occasional incorporation of defective regions within the device active layer (i.e. device ❸) and (2) when the device channel region is formed on single grains, variation in the film crystallographic orientation (i.e. devices ❶ and ❷). To improve the absolute value and the uniformity of TFT characteristics, both causes have to be addressed. Clearly, out of the two, the former cause has a more profound impact on TFT performance and uniformity.

Variation in carrier mobility with Si crystallographic orientation is well-known and is attributed to the anisotropy in the effective electron/hole mass [11]. This effect can explain electron mobility variation of up to ~150cm²/Vs between devices that happen to fall on pure

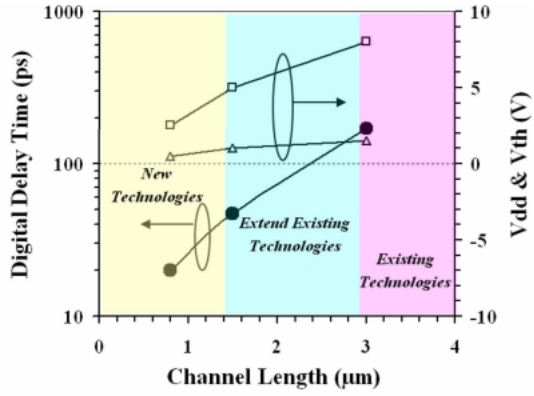

Fig. 2 Technical specifications corresponding to SOP requirements. New technologies are needed beyond the 1.5 μm design rule node.

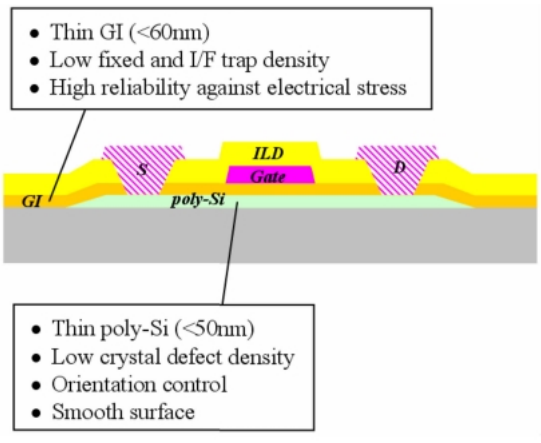

Fig. 3 Poly-Si TFT cross-section showing key device layers and associated, specific requirements.

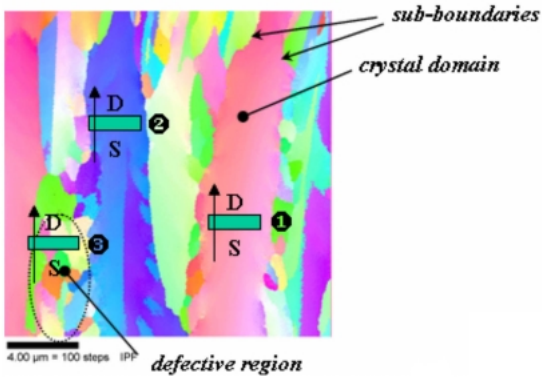

Fig. 4 Advanced poly-Si film microstructure.

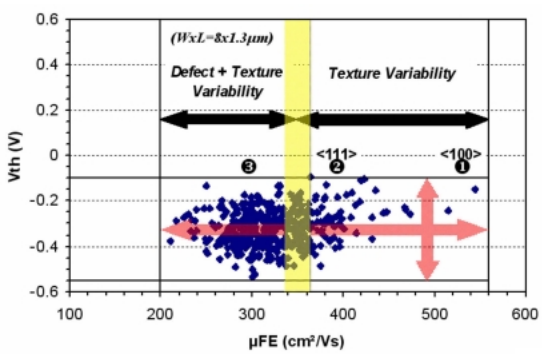

Fig. 5 Threshold voltage versus mobility for poly-Si TFTs fabricated by adv-CGSi process at SLA.

<111> or <100> regions. Further decrease in mobility is attributed to the inclusion of material defects, within the active region, in addition to crystallographic variation. It follows that the impact of material defects is more severe on performance. Therefore, to improve mobility, reduction (and ultimately elimination) of material defects is the first priority, before attacking texture variation.

Threshold voltage is also affected by crystallographic orientation, although this effect is much weaker compared to that on mobility. The effect of texture is linked to variations in the density of surface states. “Bulk” defects in the poly-Si active layer are also contributing to variations in Vth. It again appears that the latter effect (bulk defects) is stronger. In that sense, measures that reduce bulk states should be first sought to combat threshold voltage variation.

Starting from this premise, SLA has further advanced adv-CGSi process by applying a localized crystallization scheme that enables better control of the microstructure. As a result, substantial improvement on the uniformity of TFT characteristics has been achieved, as shown in **Fig. 6**.

The achieved improvement is the result of the consistently reduced defect density within the crystal region that comprises the device channel. Additional improvements, towards the set goal, are expected by employing partial (and ultimately total) texture control technologies. Such efforts are currently ongoing at SLA (for example see **Fig. 7**).

2.2. Gate Insulator Formation

Gate insulator technology is a critical area for next generation poly-Si TFTs. This is driven by the stringent requirements in GI thickness (physical or electrical equivalent) and film quality - i.e. fixed and interface trap

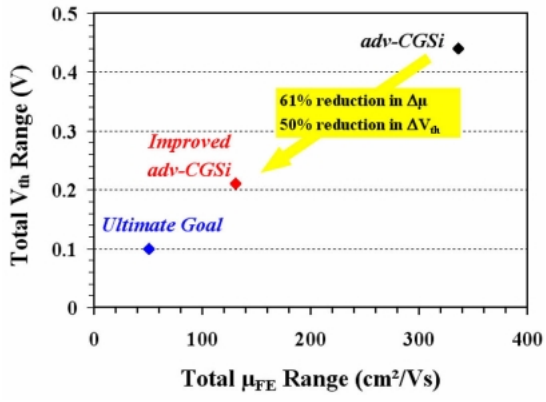

Fig. 6 Improvements in variability control of TFT characteristics by advanced adv-CGSi process family.

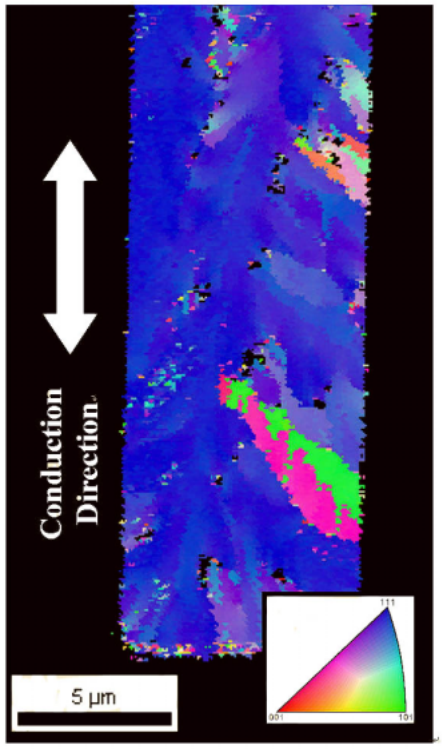

Fig. 7 EBSP image of adv-CGSi crystallized Si island showing development of preferred crystallographic orientation (see inset Kikuchi triangle for color coding).

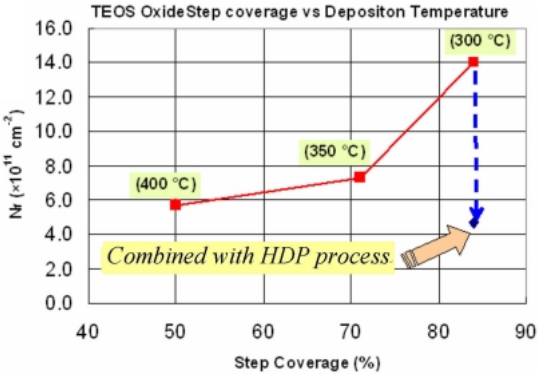

Fig. 8 Trade off between TEOS-SiO_2 step coverage and film quality (in terms of fixed-trap density) as a function of deposition temperature. New technology developed at SLA aims at resolving this trade-off in support of next generation TFT device requirements.

density. GI thickness reduction is necessitated by device scaling. An intermediate target of 50-70 nm, followed by even more drastic thickness reduction to 20-30 nm is shown in roadmaps of display device technology. As GI thickness decreases, issues of step coverage become

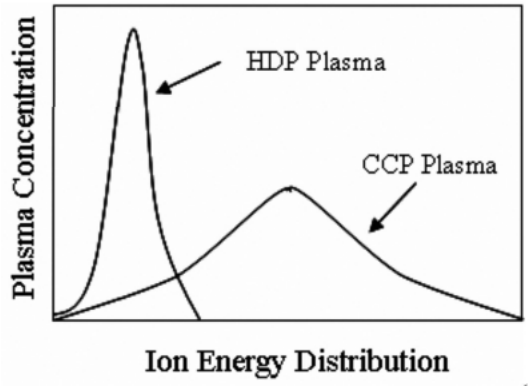

Fig. 9 Active species concentration vs. ion energy distribution comparison between conventional (CCP) plasma and high-density (HDP) plasma.

increasingly more severe. With current GI technology (based on TEOS-SiO_2) a trade off exists between film quality and step coverage. Film deposition temperature, in this case, is the key parameter. While TEOS films deposited at low temperature demonstrate excellent step coverage, they lack sufficient quality. On the flip side, high deposition temperature improves film quality, but degrades step coverage. **Fig. 8** demonstrates this trade-off.

SLA has been developing High-Density-Plasma based gate-insulator technology in support of next generation TFT requirements [12-13]. Based on the development and process optimization at SLA, superior quality dielectric films have been demonstrated, rivaling in quality that of thermal oxide. The excellent material characteristics are attributed to favorable plasma conditions that enable low plasma damage, especially around the interface region. This is, in part, explained by the ion energy distribution within the plasma configuration employed by SLA (see **Fig. 9**). Under optimal conditions we can obtain high concentration of desirable radicals, with narrow electron/ ion energy distribution. The lack of distribution "tail" into the high energy region is particularly beneficial for keeping the plasma potential low and essentially eliminating plasma damage due to ion acceleration towards the deposited film.

The proprietary HDP technology developed by SLA can be applied by itself, or in combination with conventional TEOS technology. When combined with TEOS-SiO_2, HDP process can substantially improve the combined GI characteristics. Returning to **Fig. 8**, we observe a significant reduction in fixed-states when TEOS-SiO_2 is optimally combined with HDP SiO_2. Under these conditions, excellent step coverage AND film quality can be realized. Recent data indicate that such combination has further beneficial implications, as it is even more effective than conventional annealing steps in terms of achieving uniform film characteristics. In that sense, increasing the uniformity in flat-band voltage provides a direct means for improving the uniformity of the TFT threshold voltage.

3. DEVICE TECHNOLOGY & ARCHITECTURE

In addition to developing elemental process technologies, SLA has been studying modification of the basic device architecture to enable additional degrees of freedom and strategies for performance optimization. The thrust of this activity is function-driven architecture; in other words TFT architecture is tailored according to the device function. This can be better understood by placing different device architectures on speed versus power consumption map (**Fig. 10**).

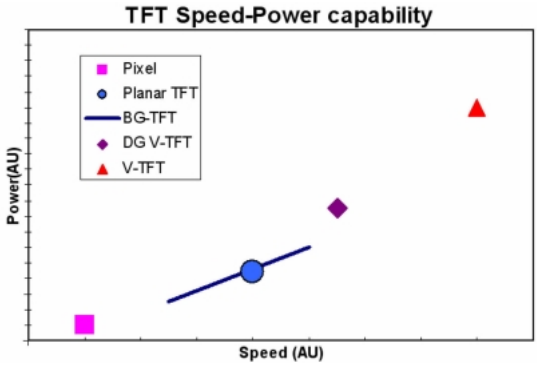

Fig. 10 Power-vs.-Speed capability for various TFT architectures.

Using a combination of different architectures on the panel we can resolve the usual trade-off between power consumption and speed. Moreover, SLA embodiments of double-gate and bottom-gate architectures are uniquely tied to advances in crystallization and gate insulator process technologies. At the very high end of the speed range, novel device concepts (dubbed "V-TFT") are being developed to enable deep-sub-µm design rules with existing (LCD) lithographic capabilities. The mixing and co-integration of different device architectures is aiming at:

1. Threshold voltage control and centering (without need of precise channel doping steps).
2. Control of hot-carrier (kink) effects (without additional drain engineering steps).
3. Integration of low-voltage and high-voltage TFTs without additional lithographic steps.

4. Realization of very high-speed TFTs for the ultimate integration of basic processing capabilities, on-panel.

Items #1 and #2 can be achieved by simple modifications of the basic, planar TFT architecture. For example, some sort of double-gate structure can be used. SLA has been researching this technology and developing proprietary architectures. Examples of Vth swings by double gate structures fabricated at SLA can be seen in **Fig. 11**. Items #3 & #4 are being addressed by novel process technologies, among which, devices featuring a unique vertical-channel architecture. A notable example is the recent fabrication of a world-first 0.25μm-channel TFT by an i-line lithography tool-set.

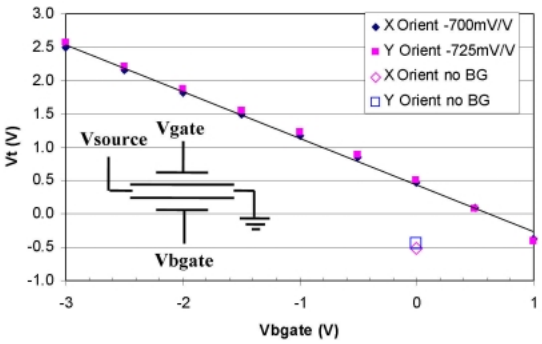

Fig. 11 nMOS TFT threshold voltage adjustment as a function of back-gate voltage.

Conclusions

SLA is developing novel process and device technologies in support to the requirements set forth for 3rd SOP generation. New crystallization and gate insulator technologies are aiming at improving the quality of the respective device layers. Novel device architectures are also being studied to complement material quality enhancement measures and provide additional controls for system optimization. Based on the overall improvement plan, SLA technology is aiming at providing solutions for high quality, new function and lower processing cost. SLA's goals are both short-term and long-term. Short term goals are focusing in supporting the implementation of new technology into pilot manufacturing. Long term goals are the identification and research of the types of display-related technologies that Sharp ought to pursue to procure the next generation of "one-of-a-kind" display products.

Acknowledgements

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